JPW

Patent Application
Attorney Docket No.: 57941.000063
Client Reference No.: RA001.2003.2.C.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael FARMWALD et al.

Appln. No.: 10/716,596

Filed: November 20, 2003

For: INTEGRATED CIRCUIT I/O USING A HIGH PERFORMANCE BUS INTERFACE

Group Art Unit: 2818

Examiner: Unassigned

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicant(s) hereby submits attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-identified patent application. Applicant(s) hereby expressly

reserves the right to swear behind the effective dates of any of the cited references. Applicant(s) further reserves the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the best references of which the associated individuals are aware.

The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicant(s).

In accordance with 37 C.F.R. § 1.98(a), only copies of the cited references which are not U.S. patents or U.S. patent application publications are being submitted herewith. However, copies of the cited references which are U.S. patents or U.S. patent application publications will be submitted at the request of the Examiner. In considering these cited references, it may be noted by the Examiner that certain of the references may

contain markings, underlinings, and/or other notations. These markings, underlinings, and/or other notations are not to be construed as drawing the Examiner's attention either to selected parts or away from other parts of these cited references. Any such markings were either present on the copies of these cited references when obtained by the associated individuals, or were made thereon during the study of these cited references by the associated individuals.

In accordance with 37 C.F.R. § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified patent application entered the national stage as set forth in 37 C.F.R. § 1.491; (iii) before the mailing date of a first Office Action on the merits for the above-identified patent application; or (iv) before the mailing date of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

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Respectfully submitted,

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Date: January 21, 2005

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.: 57941.000063	SERIAL NO.: 10/716,596
		INVENTOR'S NAME: Michael FARMWALD et al.	EXAMINER: Unassigned
	LIST OF MATERIALS CITED BY APPLICANT	FILING DATE: November 20, 2003	GROUP: 2818
	(Use several sheets if necessary)		

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	1.	4360870	11/23/1982	McVey			
	2.	4379222	04/05/1983	Hayter et al.			
	3.	4394753	07/19/1983	Penzel			
	4.	4494021	01/15/1985	Bell et al.			
	5.	4506348	03/19/1985	Miller			
	6.	4513372	04/23/1985	Ziegler et al.			
	7.	4520465	05/28/1985	Sood			
	8.	4562435	12/31/1985	McDonough et al.			
	9.	4597019	06/24/1986	Nishimoto et al.			
	10.	4628489	12/09/1986	Ong			
	11.	4637018	01/13/1987	Flora			
	12.	4688197	08/18/1987	Novak et al.			
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	14.	4755937	07/05/1988	Glier			
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	17.	4811364	03/07/1989	Sager et al.			
	18.	4849937	07/18/1989	Yoshimoto			
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	20.	5001672	03/19/1991	Ebbers			
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	22.	5134699	07/28/1992	Aria et al.			
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						Yes	No
	24.	02197553	05/18/1988	GB			
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	27.	6443894	02/16/1989	JP			

EXAMINER	DATE CONSIDERED

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		OTHER MATERIALS (Including Author, Title, Date, Pertinent Pages, Etc.)
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	29.	Gustavson, David B., 11/28/1988, SCI-C [1 and SCI 2], Scalable Coherent Interface
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	31.	Johnson, Mark G; Hudson, Edwin L., IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, 10/00/1988, Johnson (IEEE 10/88), A Variable Delay Line PLL For CPU- Coprocessor Synchronization
	32.	Intel, Intel Publication Number 171873-001 Rev. A, 1981, iAPX432 GDP Datasheet, Intel iAPX43202 VLSI General Data Processor Data Sheet
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	37.	Watanabe, S. et. al., IEEE Journal of Solid State Circuits, vol. 24 No. 3, p. 763, 06/00/1982, An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial Read/Write Mode
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	39.	JEDEC, JC 42.3 Committee On MOS Memories, 09/14/1988, Minutes Of Meeting No. 47 JC-42.3 Committee On MOS Memories w/Attachment L (Proposal)
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	42.	JEDEC, JC 42.3 Committee On MOS Memories, 12/06/1989, Minutes Of Meeting No. 52 JC 42.3 Committee On MOS Memories w/Attachment K
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	45.	Patterson, David A. et al., Morgan Kaufmaim Publishers, Inc., San Francisco, CA 1996, Computer Architecture A Quantitative Approach (Second Edition), excerpts
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		OTHER MATERIALS (Including Author, Title, Date, Pertinent Pages, Etc.)
	49.	Lidington, Gary P., Digital Technical Journal, No. 7, August 1988, pp. 79-86, Overview of the MicroVAX 3500/3600 Processor Module
	50.	Copy of Hynix's Amended Supplemental Revised Preliminary Invalidity Contentions
	51.	PATTERSON et al., Computer Architecture A Quantitative Approach
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